IN THE CLAIMS

No amendments to the claims are requested. The currently-pending claims are:

1. (Previously Presented) A method comprising:

maintaining a first page table map for use in an isolated execution mode and a second page table map for use in a normal execution mode;

restricting access to an isolated area of memory to bus cycles performed in the isolated execution mode;

dynamically swapping between the first page table map and the second page table map responsive to a change in execution mode;

identifying if an event is one of a class of events to be handled in the isolated execution mode;

asserting a selection signal to select the first page table map if the event is identified as one of the class of events to be handled in the isolated execution mode; and

handling the event using a table map selected by the selection signal.

2. (Previously Presented) The method of claim 1 further comprising:

identifying if the event is one of a class of events to be handled in the isolated execution mode; and

handling the event using the first page table map if the event is identified as one of the class of events to be handled in the isolated execution mode;

wherein identifying comprises indexing into a lookup table with a exception vector of the event.

3. (Original) The method of claim 1 wherein dynamically swapping comprises:

loading a set of control registers selected based on an exception vector of the event.

4. (Original) The method of claim 3 wherein the set of control registers comprises:

a global descriptor table register;

an interrupt descriptor table register; and

a page table map base address register.

5. (Original) The method of claim 1 wherein maintaining comprises:

mirroring a page table base address register.

6. (Original) The method of claim 1 further comprising:

defining a set of events that should be handled in isolated execution mode.

7. (Original) The method of claim 6 wherein the set of events to be handled in the isolated execution mode comprises:

machine check events and clock events.

8. (Previously Presented) The method of claim 1 wherein handling comprises:

determining if a current mode is the isolated execution mode;

loading a set of control registers with values corresponding to the first page table map if the current mode is not the isolated execution mode and the event is one of the class; and

dispatching an exception vector after the loading is complete.

9. (Previously Presented) An apparatus comprising:

a first storage location storing control data for a first page table map;

a second storage location storing control data for a second page table map;

a selection unit to select which page table map is applied responsive to receipt of an event; and

an isolated execution circuit to generate isolated access bus cycles,

wherein isolated access bus cycles are to be used if the apparatus operates in an isolated execution mode.

10. (Original) The apparatus of claim 9 wherein the selection unit comprises:

a multiplexer that selects between the first and the second storage locations based on an exception vector of the event.

11. (Original) The apparatus of claim 9 wherein the first storage location contains a base address for the first page table map and the second storage location contains a base address for the second page table map.

12. (Previously Presented) A platform comprising:

a processor executing in one of normal execution mode and isolated execution mode;

a first set of control registers to define a current memory map of the platform;

a mapping unit to dynamically load the first set of control registers responsive to an event if the event should be handled using an alternate memory map; and

an isolated execution circuit to generate isolated access bus cycles if the processor is executing in the isolated execution mode.

13. (Original) The platform of claim 12 wherein the mapping unit comprises:

a second set of registers having a first subset corresponding to control register values for a normal execution mode memory map and a second subset corresponding to control register values for an isolated execution mode memory map; and

a selection unit to select between the first subset and the second subset.

14. (Original) The platform of claim 13 wherein the selection unit comprises:

a plurality of multiplexers having selection driven by an exception vector of an incoming event.

15. (Original) The platform of claim 12 wherein the first set of control registers comprises:

a global descriptor table register;

an interrupt description table register; and

a page table map base address register.

16. – 30. (Canceled)